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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,250	12/31/2003	Billy K. Taylor	INT-12	3843

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,250	TAYLOR ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *17-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-16, drawn to a first firmware program initializing a first interrupt table for a first list of devices and a second firmware program initializing a second interrupt table for a second list of devices, classified in class 713, subclass 2.

   II. Claims 17-21, drawn to partitioning of the system having connectors coupled to a bus, classified in class 716, subclass 6.

   III. Claims 22-27, drawn to interrupt processing in a plurality of domains, classified in class 710, subclass 260.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct form each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a first firmware program initializing a first interrupt table for a first list of devices without the need of partitioning of the system having connectors coupled to a bus. See MPEP § 806.05(d).

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct form each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a first firmware program initializing a first interrupt table for a first list of devices without the need of interrupt processing in a plurality of domains. See MPEP § 806.05(d).

Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct form each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as partitioning of the system having connectors coupled to a bus without the need of interrupt processing in a plurality of domains. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II and III, the search required for Group II is not required for Group I and III, the search required for Group III is not required for Group I and II, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Carrie A. Boone on May 18, 2006, a provisional election was made with traverse to prosecute the invention of Group I, claims 1-16. Affirmation of this election must be made by applicant in replying to this office action. Claims 17-27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Corrigan et al (US Patent 6,772,259; hereinafter Corrigan).

8. As per claim 1, AAPA discloses a partitionable system, comprising:

a first domain [pages 1-2; a multiprocessor system supporting multiple domains];

a second domain [pages 1-2; a multiprocessor system supporting multiple domains];

wherein the system is partitionable into the first domain and the second domain [pages 1-2; a multiprocessor system supporting multiple domains]; and

a plurality of input/output devices [pages 1-2; each domain may include input/output (I/O) devices and other modules, such that each domain operates wholly independent of other domains; the independent operations include the execution of programs such as firmware].

AAPA does not expressly disclose about having separate interrupt tables for each domain. However, Corrigan clearly discloses the problem, which arises in the context of partitioned and non-partitioned environments, is that the interrupt handler must be coded differently for each environment. Corrigan solves the problem by providing separate interrupt tables [col. 1, lines 59-65; col. 2, lines 33-41; col. 2, line 66 -- col. 3, line 5; col. 3, lines 50-54; col. 9, lines 48-59]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to a multiprocessor system having partitioned and unpartitioned systems. Moreover, Corrigan clearly provides the solution for unused but physically present input/output devices in an unpartitioned system by having a different interrupt table for partitioned and unpartitioned system.

9. As per claim 2, AAPA discloses that the first processor is interrupted by the first single-instance and the first multi-instance devices and the second processor is interrupted by the second single-instance and the second multi-instance devices [pages 1-2; inherent to the partitioned system into several domains].

10. As per claim 3, AAPA discloses that a first operating system is booted in the first domain and a second operating system is booted in the second domain when the system is partitioned [pages 1-2].

11. As per claim 4, AAPA discloses that the first operating system is a legacy operating system [pages 1-2].

12. As per claim 5, AAPA discloses that the domain operates wholly independent of other domains and the independent operations include the execution of programs such as firmware [pages 1-2]. AAPA does not expressly disclose about having separate interrupt tables for each domain. However, Corrigan clearly discloses the problem, which arises in the context of partitioned and non-partitioned environments, is that the interrupt handler must be coded differently for each environment. Corrigan solves the problem by providing separate interrupt tables [col. 1, lines 59-65; col. 2, lines 33-41; col. 2, line 66 -- col. 3, line 5; col. 3, lines 50-54; col. 9, lines 48-59]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to a multiprocessor system having partitioned and unpartitioned systems. Moreover, Corrigan clearly provides the solution for unused but physically present input/output devices in an unpartitioned system by having a different interrupt table for partitioned and unpartitioned system.

13. As per claim 6, AAPA discloses that the first processor is interrupted by the first single-instance, the first multi-instance, or the second multi-instance devices [pages 1-2; inherent to the partitioned system].

14. As per claim 7, AAPA discloses that the second processor is interrupted by the first single-instance, the first multi-instance, or the second multi-instance devices [pages 1-2; inherent to the partitioned system].

15. As per claim 8, AAPA discloses that the second single-instance devices are unused [pages 12; unused but physically present input/output device in an unpartitioned state].

16. As per claim 9, Corrigan discloses use of registers for indication of partitioned or unpartioned state[col. 3, line 61 -- col. 4, line 21].

17. As per claim 10, AAPA discloses that an interrupt controller accessible to the first domain and to the second domain [pages 1-2; inherent to the system partitioned in domains].

18. As per claim 11, AAPA discloses that the first interrupting device receives the first processor interrupt and the second interrupting device receives the second processor interrupt when the system is not partitioned [pages 1-2; inherent to the system].

19. As per claims 14-16, the use of a reset handler in a multiprocessor system having partitioned and unpartitioned systems is inherent [pages 1-2].

20. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Corrigan et al (US Patent 6,772,259; hereinafter Corrigan) in view of Kim (US Patent 6,952,749).

21. As per claims 12-13, AAPA and Corrigan disclose the invention substantially. AAPA and Corrigan do not disclose about use of a multiplexer for routing interrupts. However, Kim clearly discloses use of multiplexers in routing the interrupts [Fig. 3; col. 11, lines 37-41]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they all are somewhat directed to an interrupt handling system for a multiple processor system. Moreover, use of a multiplexer would clear be the easiest and convenient way of selectively directing the interrupt to an appropriate processor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
May 18, 2006

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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